HP 1660E/ES/EP Series Logic Analyzer key Specifications and Characteristics

HP Model Number	1660E/ES/EP	1661E/ES/EP	1662E/ES/EP	1663E/ES/EP	1664A
State and Timing Channels	136	102	68	34	34
Timing Analysis	Conventional: 250 MHz all channels, 500 MHz half channels Transitional: 125 MHz all channels, 250 MHz half channels Glitch: 125 MHz half channels				
State analysis speed	100 MHz, all channels				50 MHz
State Clock/Qualifiers	6	6	4	2	2
Memory Depth per Channel	4k per channel, 8k in half-channel modes				
LAN Port	Standard for all E/ES/EP models				N/A

HP 1660EP Series Pattern Generator Key Specifications and Characteristics

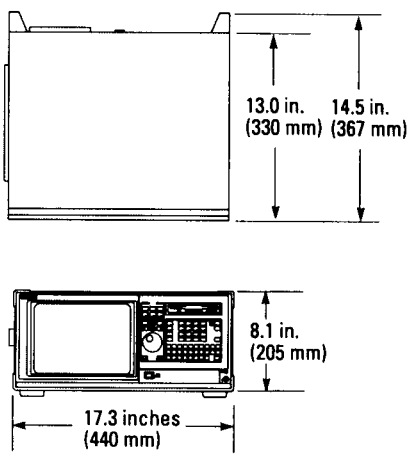
HP Model Number	1660EP, 1661EP, 1662EP, 1663EP		
Maximum Clock Speed	200 MHz	100MHz	50 MHz
Number of Data Channels	16	32	32
Memory Depth, in vectors	258,048	258,048	258,048
"IF" Command	No	No	Yes

HP 1670E-Series Logic Analyzer Key Specifications and Characteristics

HP Model Number	1670E	1671E	1672E
State and Timing Channels	136	102	68
Timing Analysis	Conventional: 125 MHz all channels, 250 MHz half channels		
State Analysis Speed	100 MHz, all channels		
State Clocks/ Qualifiers	4	4	4
Memory Depth per Channel	1M per channel, 2M in timing half-channel mode		

HP 1660ES Series Oscilloscope Key Specifications and Characteristics

HP Model Number	1660ES, 1661ES 1662ES, 1663ES
Channels	2
Maximum Sample Rate	2 GSa/s per channel
Bandwidth	dc to 500 MHz (dc coupled)
Rise Time	700 ps
Vertical Resolution	8 bits
Memory Depth per Channel	32k samples



Weight = 28.6 lbs. (13kg)

Figure 3. Logic analyzer dimensions and weight

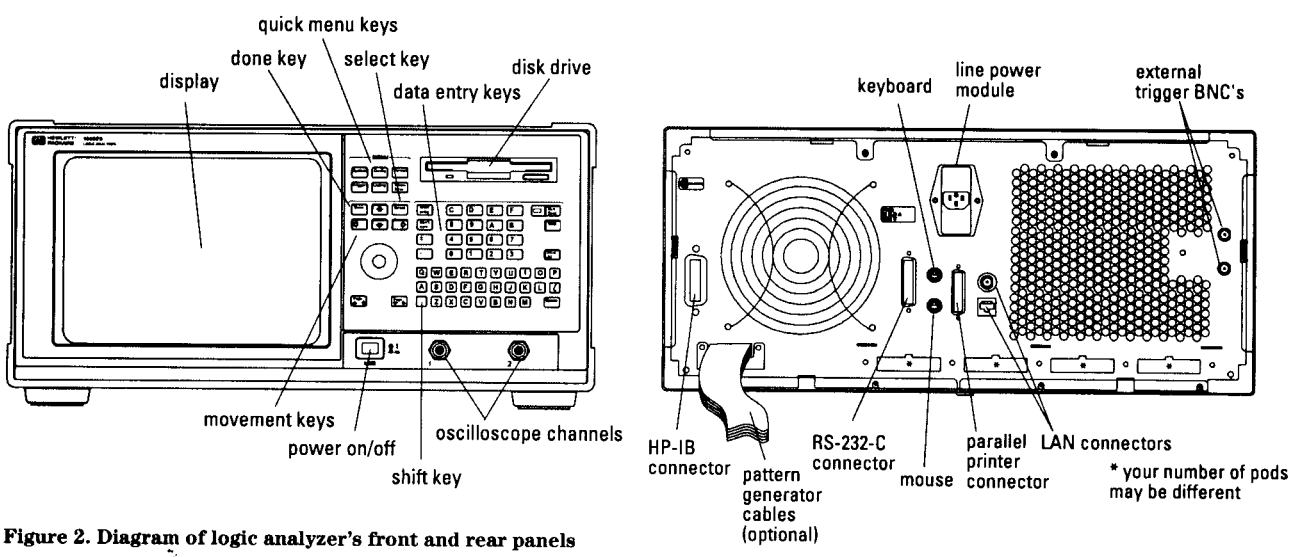


Figure 2. Diagram of logic analyzer's front and rear panels

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics

Human Interface

Front Panel A knob and keypad make up the front-panel human interface. Keys include control, menu, display navigation, and alpha-numeric entry functions.

Mouse A DIN mouse is shipped as standard equipment. It provides full instrument control. Knob functionality is replicated by holding down the right button and moving the mouse left or right. [1]

Keyboard The logic analyzer can also be operated using a DIN keyboard. Order the HP Logic Analyzer Keyboard Kit, model number HP E2427B. [1]

Input/Output, Control, and Printing

I/O Ports All units ship with a Centronics parallel printer port, RS-232, and HP-IB as standard equipment.

LAN Interface An Ethernet LAN interface is standard. The LAN interface comes with both Ethertwist and ThinLan connectors. The LAN supports FTP and PC/NFS connection protocols. It also works with X11 windows packages. [1]

Programmability Each instrument is fully programmable from a computer via HP-IB, RS-232 and LAN connections. [1]

HP Printer Support Printers which use the HP Printer Control Language (PCL) and have a parallel Centronics, RS-232 or HP-IB interface are supported:
HP DeskJet, LaserJet, QuietJet, PaintJet, and ThinkJet models

Alternate Printers Supported The Epson FX80, LX80 and MX80 printers with an RS-232 or Centronics interface are supported in the Epson 8-bit graphics mode.

Hard Copy Output Screen images can be printed in black and white or color from all menus using the *Print* field. State or timing listings can be also be printed in full or part (starting from center screen) using the *Print All* selection.

Mass Storage Files and Software

Updating the Operating System The operating system resides in Flash ROM and can be updated from the flexible disk drive or from the internal hard disk drive. [1]

Mass Storage Supported by an internal hard disk drive and by a 1.44 Mbyte, 3.5-inch flexible disk drive. Supports DOS and LIF formats. [1]

Screen Image Files An image file of any display screen can be stored to disk via the display's *Print* field in black & white or color TIFF, color PCX, or black & white Encapsulated PostScript™ (EPS) formats.

ASCII Data Files State or timing listings can be stored as ASCII files on a disk via the display's *Print* field. These files are equivalent in character width and line length to hard-copy listings printed via the *Print All* selection.

Configuration and Data Files Logic analyzer and oscilloscope files that include configuration and data information (if present) are encoded in a binary format. They can be stored to or loaded from the hard disk drive or a flexible disk.

Recording of Acquisition and Storage Times Binary format configuration/data files are stored with the time of acquisition and the time of storage. [1]

Acquisition Arming

Initiation Arming is started by *Run, Group Run,* or the Port In BNC.

Cross Arming Analyzer machines and the oscilloscope or pattern generator can cross-arm each other.

Output An output signal is provided at the Port Out BNC.

PORT IN Signal and Connection Port In is a standard BNC connection. The input operates at TTL logic signal levels. Rising edges are valid input signals.

PORT OUT Signal and Connection Port Out is a standard BNC connection with TTL logic signal levels. A rising edge is asserted as a valid output.

Skew Adjustment Correction factors for nominal skew between displayed timing and oscilloscope signals are built into the operating system. Additional correction for unit-by-unit variation can be made using the *Skew* field. An entered skew value affects the next (not the present) acquisition display.

1] Please refer to HP 1664A Product Specifications and Characteristics on page 7.

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

PORT IN Arms Logic Analyzer [2]	15 ns typical delay from signal input to a *don't care* logic analyzer trigger.
PORT IN Arms Oscilloscope	40 ns typical delay from signal input to an *immediate* oscilloscope trigger.
Logic Analyzer Arms PORT OUT [2]	120 ns typical delay from logic analyzer trigger to signal output.
Oscilloscope Arms PORT OUT	60 ns typical delay from oscilloscope trigger to signal output.

Operating Environment

Power	115 Vac or 230 Vac, –22% to +10%, single phase, 48-66 Hz, 320 VA max
Temperature	Instrument, 0° to 50° C (+32° to 122° F). Disk media, 10° to 40° C (+50° to 104°F). Probes and cables, 0° to 65° C (+32° to 149° F)
Humidity	Instrument, up to 95%, relative humidity at +40° C (+140° F). Disk media and hard drive, 8% to 85% relative humidity.
Altitude	To 3,048 m (10,000 ft) [1]
Vibration: Operating	Random vibrations 5–500 Hz, 10 minute per axis, ~ 0.3 g (rms).
Vibration: Non Operating	Random vibrations 5–500 Hz,10 minutes per axis,~ 2.41 g (rms); and swept sine resonant search, 5–500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

[1] Please refer to HP 1664A Product Specifications and Characteristics on page 7.

[2] Time may vary depending upon the mode of logic analyzer operation.

* Warranted specification.

[3] Full channel /half channel modes

Physical Factors

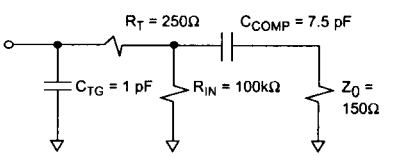
Safety	IEC 348/ HD 401, UL 1244, and CSA Standard C22.2 No. 231 (series M-89)

EMC

CISPR 11:1990/EN 55011 (1991): Group 1 Class A
IEC 801-2:1991/EN 50082-1 (1992): 4kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m
IEC 801-4:1988/EN 50082-1 (1992): 1kV

Logic Analyzer Probes

Input Resistance	100 kΩ ±2%
Input Capacitance	approx. 8 pF (see figure 4)



High Frequency Model for Probe Inputs

Figure 4

Minimum Input Voltage Swing	500 mV peak-to-peak
Minimum Input Overdrive	250 mV or 30% of input amplitude, whichever is greater
Threshold Range	–6.0 V to +6.0 V in 50-mV increments
Threshold Setting	Threshold levels may be defined for pods (17-channel groups) on an individual basis
Threshold Accuracy*	± (100 mV +3% of threshold setting)
Input Dynamic Range	± 10 V about the threshold
Maximum Input Voltage	± 40 V peak
+5 V Accessory Current	1/3 amp maximum per pod
Channel Assignment	Each group of 34 channels (a pod pair) can be assigned to Machine 1, Machine 2 or remain unassigned. The HP 1663E/ES/EP and the HP 1664A do not have a Machine 2.

State Analysis

Maximum State Speed*	100 MHz[1] all models
Memory Depth per Channel	
HP 1660E/ES/EP Series	4k samples std. Time tags on: 2k samples
HP 1670E Series	1M samples standard Time Tags On: 500k samples Compare Mode On: 250k samples Compare Mode and Time Tags On: 120k samples
State Clocks	Clock edges can be ORed together and operate in single phase, two-phase demultiplexing, or two-phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.
State Clock Qualifier	The high or low voltage level of up to 4 of the 6 clocks can be ANDed or ORed with the clock specification.

Setup/Hold* [4]

one clock, one edge	3.5/0 ns to 0/3.5 ns (in 0.5 ns increments)
one clock, both edges	4.0/0 ns to 0/4.0 ns (in 0.5 ns increments)
multi-clock, multi-edge	4.5/0 ns to 0/4.5 ns (in 0.5 ns increments)

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

Minimum State Clock Pulse Width* [4]	3.5 ns
Minimum Master to Master Clock Time* [4]	10.0 ns
Minimum Slave to Slave Clock Time [4]	10.0 ns
Minimum Master to Slave Clock Time [4]	0.0 ns
Minimum Slave to Master Clock Time [4]	4.0 ns
Clock Qualifiers Setup/Hold [4]	4.0/0 ns (fixed)
State Tagging [5]	Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Max. count is 4.29×10^9.
Time Tagging [5]	Measures the time between stored states, relative to either the previous state or to the trigger. Max. time between states is 34.4 sec. Min. time between states is 8 ns.
Time Tag Resolution	8 ns or 0.1% (whichever is greater)

Timing Analysis

Conventional Timing	Data stored at selected sample rate across all timing channels.

HP 1660 Series

Sample Period [3]	4 ns/2 ns minimum, 8.38 ms maximum

HP 1670 Series

Sample Period [3]	8 ns/4 ns minimum, 41 ms/10 ms maximum
Time Covered by Data [3]	Sample period × memory depth
Transitional Timing	(HP 1660E/ES/EP Series only) Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.
Time Covered by Data [3]	16.3 µs minimum, 9.7 hrs./6.5 hrs. maximum
Maximum Time Between Transitions	34.4 s
Number of Captured Transitions [3]	1023-2047/682-4094 Depending on input signals
Glitch Capture Mode	(HP 1660E/ES/EP Series only.) Data sample and glitch information is stored every sample period.
Maximum Timing Speed	125 MHz
Sample Period	8 ns minimum, 8.38 ms maximum
Minimum Glitch Width*	3.5 ns
Maximum Glitch Width	Sample Period – 1 ns
Memory Depth per Channel	2048 samples
Time Covered by Data	Sample Period × 2048: 16.3 µs minimum, 17.1 sec maximum

Time Interval Accuracy

Sample Period Accuracy	± 0.01%
Channel-to-Channel Skew	2 ns typical, 3 ns maximum
Time Interval Accuracy	± (Sample Period Accuracy + channel-to-channel skew + 0.01% of time interval reading)
Maximum Delay After Triggering	Sample Period 2-8 ns : 8.389 ms Sample Period > 8 ns: 1,048,575 × sample period

Trigger Specifications

Trigger Macros	Trigger setups can be selected from a categorized list of trigger macros. Each macro is shown in graphical form and has a written description. Macros can be chained together to create a custom trigger sequence.
Pattern Recognizers	Each recognizer is the AND combination of bit (0,1, or X) patterns in each label. Ten pattern recognizers are available.
Minimum Pattern and Range Recognizer Pulse Width	>125 MHz timing modes: 13 ns + channel-to-channel skew ≤125 MHz timing modes: 1.01 x (1 sample period +1 ns + channel-to-channel skew)

[3] Full Channel /Half Channel Modes

[4] Specified for an input signal VH= – 0.9V, VL = – 1.7V, slew rate = 1V/ns, and threshold = –1.3V

[5] Time or-state-tagging (Count Time or Count State) is available in the full-channel state mode. There is no speed penalty for tag use. Memory is halved when time or state tags are used unless a pod pair (34-channel group) remains unassigned in the Configuration menu.

* Warranted specification.

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

Range Recognizers	Recognize data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones). Two range recognizers are available.
Range Width	32 channels
Edge/Glitch Recognizers	Trigger on glitch or edge on any channel. Edge can be specified as rising, falling or either.
Edge/Glitch Recognizers	2 (in timing mode only)
Edge/Glitch Recovery Time	Sample Period 2-8 ns: 28 ns Sample Period > 8 ns: 20 ns + sample period
Qualifier	A user-specified term that can be any state, no state, any recognizer, (pattern, ranges or edge/glitch), any timer, or the logical combination (NOT, AND, NAND, OR, NOR, XOR, NXOR) of the recognizers and timers.
Branching	Each sequence level has a branching qualifier. When satisfied, the analyzer will branch to the sequence level specified.
Occurrence Counters	Qualifiers may be specified to occur up to 1,048,575 times before advancing to the next level. Each sequence level has its own counter. The maximum occurrence count is 1,048,575.
Storage Qualification (state only)	Each sequence level has a storage qualifier that specifies the states that are to be stored.

Maximum Sequencer Speed	125 MHz
State Sequence Levels	12
Timing Sequence Levels	10
Timers	Timers may be Started, Paused, or Continued at entry into any sequence level after the first.
Timers	2
Timer Range	400 ns to 500 seconds
Timer Resolution	16 ns or 0.1% whichever is greater
Timer Accuracy	± 32 ns or ± 0.1%, whichever is greater
Timer Recovery Time	70 ns

Acquisition, Measurement and Display Functions

Run	Starts acquisition of data in specified trace mode.
Stop	In single trace mode or the first run of a repetitive acquisition, stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, stop halts acquisition of data and does not change current display.
Trace Mode	Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until pattern time interval or compare stop criteria are met.

Trigger	Displayed as a vertical dashed line in the timing waveform, state waveform and X-Y chart displays and as line 0 in the state listing and state compare displays.
Activity Indicators	Provided in the Configuration, State Format, and Timing Format menus for monitoring device-under-test activity while setting up the analyzer.
Labels	Channels may be grouped together and given a 6-character name called a *label*. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label. Trigger terms may be given an 8-character name.

Measurement Functions

Markers	Two markers (x and o) are shown as dashed lines in the display.
Time Intervals	The x and o markers measure the time interval between events occurring on one or more waveforms or states (available in state when time tagging is on).
Delta States	The x and o markers measure the number of tagged states between any two states (state only).
Patterns	The x or o marker can be used to locate the nth occurrence of a specified pattern before or after trigger. The o marker can also find the nth occurrence of a pattern before or after the x marker.

HP 1660E and 1670E-Series Logic Analyzer Specifications and Characteristics (cont.)

Statistics	x to o marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum x to o time, maximum x to o time, average x to o time, and ratio of valid runs to total runs.
Compare Mode Functions	Performs post-processing bit-by-bit comparison of the acquired state data and compare image data.
Compare Image	Created by copying a state acquisition into the compare image buffer. Allows editing of any bit in the compare image to a 1, X or 0.
Compare Image Boundaries	Each channel (column) in the compare image can be enabled or disabled via bit masks in the compare image. Upper and lower ranges of states (rows) in the compare image can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.
Stop Measurement	Repetitive acquisitions may be halted when the comparison between the current state acquisition and the current compare image is equal or not equal.
Compare Mode Displays	Reference Listing display shows the compare image and bit masks; difference listing display highlights differences between the current state acquisition and the compare image.

Data Display

Display Modes	State listing, state waveforms, state chart, state compare listing, compare difference listing, timing waveforms, timing listing, interleaved time-correlated listing of two state analyzers (time tags on), and time-correlated state listing with timing waveforms on the same display.
State X-Y Chart Display	Plots value of a specified label (on y-axis) versus states or another label (on x-axis). Both axes can be scaled.
State Waveform Display	Displays state acquisitions in waveform format.
Timing Listing Display	Displays timing acquisition in listing format.
Timing Waveform Display	
Accumulate	Waveform display is not erased between successive acquisitions.
Overlay Mode	Multiple channels can be displayed on one waveform display line. When waveform size is set to large, the value represented by each waveform is displayed inside the waveform in the selected base.
Displayed Waveforms	24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.
Bases	Binary, octal, decimal, hexadecimal, ASCII (display only), user-defined symbols, two's complement.
Symbols	
Pattern Symbols	User can define a mnemonic for the specific bit pattern of a label. When data display is "Symbol", mnemonic is displayed where the bit pattern occurs.
Range Symbols	User can define a mnemonic covering a range of values.
Symbol Utility	Symbolic information extracted from popular object module formats can also be used.
Number of Symbols	1000 maximum.
System Performance Analysis	SPA includes state histogram, state overview and time interval measurements to aid in the software optimization process. These tools provide a statistical overview of your synchronous design.

The HP 1664A Specifications and Characteristics

The HP 1664A is a low-cost version of the HP 1660E/ES/EP-series logic analyzer family. The HP 1664A has some specifications and characteristics that are different from the HP 1660E/ES/EP-series logic analyzers.

The HP 1664A:

- Supports a maximum of 50 MHz state acquisition
- Weight 26 pounds (11.8 kg)
- Altitude To 15,000 ft (4,752 m)
- Boots from the floppy disk drive—it does not have flash ROM
- It cannot be upgraded to include an oscilloscope or pattern generator
- The mouse and keyboard connectors are HP HIL standard
- For the optional keyboard order HP E2427A
- It does not support the symbol utility
- It does not support the software performance analysis (SPA) software
- It does not have a real time clock
- It does not have a hard disk drive
- It does not have a LAN port